Chapter 3

Circuit Models of Nonlinear Inhibition

The silicon models of auditory localization and pitch perception, presented in Chapters 4 and 5, use inhibitory processing to improve the selectivity of their output representations. This chapter describes the inhibitory processing used in these projects.

Two general types of inhibition mediate activity in neural systems: subtractive inhibition, which sets a zero level for the computation, and multiplicative (nonlinear) inhibition, which regulates the gain of the computation. The circuit described in the chapter implements general nonlinear inhibition in its extreme form, known as *winner-take-all*. In addition to the projects in Chapters 4 and 5, the winner-take-all circuit has been used successfully in a model of visual stereopsis (Mahowald and Delbruck, 1989).

The chapter also describes a modification to this global winner-take-all circuit, which computes local nonlinear inhibition. The circuit allows multiple winners in the network, and is well suited for use in systems that represent a feature space topographically and that process several features in parallel. The research in this chapter was done in collaboration with Sylvie Ryckebusch, M. A. Mahowald, and Carver Mead; parts of this chapter were originally published in (Lazzaro *et al.*, 1988).

3.1 The Winner-Take-All Circuit

Figure 3.1 is a schematic diagram of the winner-take-all circuit. Each neuron receives a unidirectional current input I_k; the output voltages $V_1 \ldots V_n$ represent the results of the winner-take-all computation. A single wire, associated with the potential V_c, computes the inhibition for the entire circuit; for an n-neuron circuit, this wire is $O(n)$ long. To compute the global inhibition, each neuron k contributes a current onto this common wire, using transistor T_{2_k}. To apply this global inhibition locally, each neuron responds to the common wire voltage V_c, using transistor T_{1_k}. This computation is continuous in time; no clocks are used. The circuit exhibits no hysteresis, and operates with a time constant related to the size of the largest input. The output representation of the circuit is not binary; the winning output encodes the logarithm of its associated input.

A static and dynamic analysis of the two-neuron circuit illustrates these properties. Figure 3.2 shows a schematic diagram of a two-neuron winner-take-all circuit. To understand the behavior of the circuit, we first consider the input condition $I_1 = I_2 \equiv I_m$. Transistors T_{1_1} and T_{1_2} have identical potentials at gate and source, and are both sinking I_m; thus, the drain potentials V_1 and V_2 must be equal. Transistors T_{2_1} and T_{2_2} have identical source, drain, and gate potentials, and therefore must sink the identical current $I_{c_1} = I_{c_2} = I_c/2$. In the subthreshold region of operation, the equation $I_m = I_o \exp(V_c/V_o)$ describes transistors T_{1_1} and T_{1_2}, where I_o is a fabrication parameter, and $V_o = kT/q\kappa$. Likewise, the equation $I_c/2 = I_o \exp((V_m - V_c)/V_o)$, where $V_m \equiv V_1 = V_2$, describes transistors T_{2_1} and T_{2_2}. Solving for $V_m(I_m, I_c)$ yields

$$V_m = V_o \ln(\frac{I_m}{I_o}) + V_o \ln(\frac{I_c}{2I_o}). \tag{3.1}$$

Thus, for equal input currents, the circuit produces equal output voltages; this behavior is desirable for a winner-take-all circuit. In addition, the output voltage V_m logarithmically encodes the magnitude of the input current I_m.

The input condition $I_1 = I_m + \delta_i$, $I_2 = I_m$ illustrates the inhibitory action of the circuit. Transistor T_{1_1} must sink δ_i more current than in the previous example; as a result, the gate voltage of T_{1_1} rises. Transistors T_{1_1} and

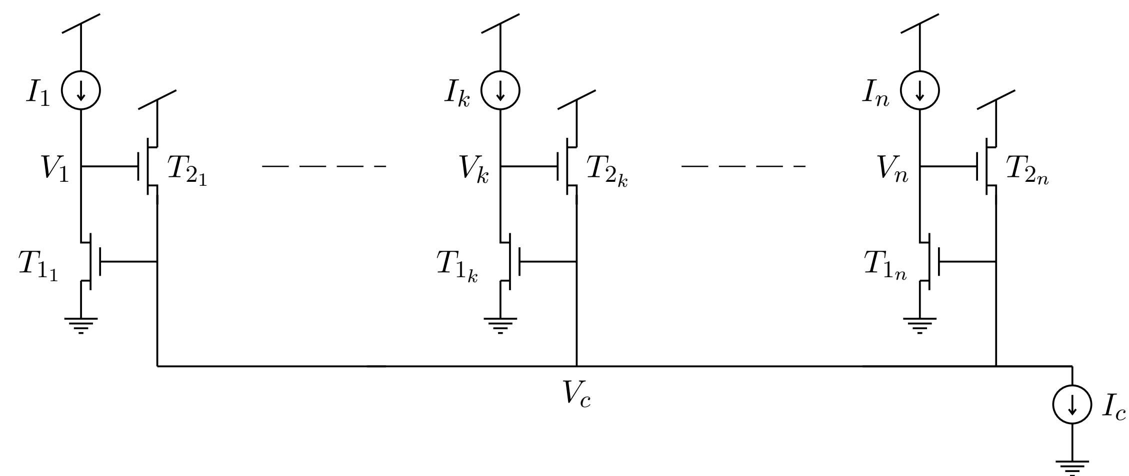

Figure 3.1. Schematic diagram of the winner-take-all circuit. Each neuron receives a unidirectional current input I_k; the output voltages $V_1 \ldots V_n$ represent the result of the winner-take-all computation. If $I_k = \max(I_1 \ldots I_n)$, then V_k is a logarithmic function of I_k; if $I_j \ll I_k$, then $V_j \approx 0$.

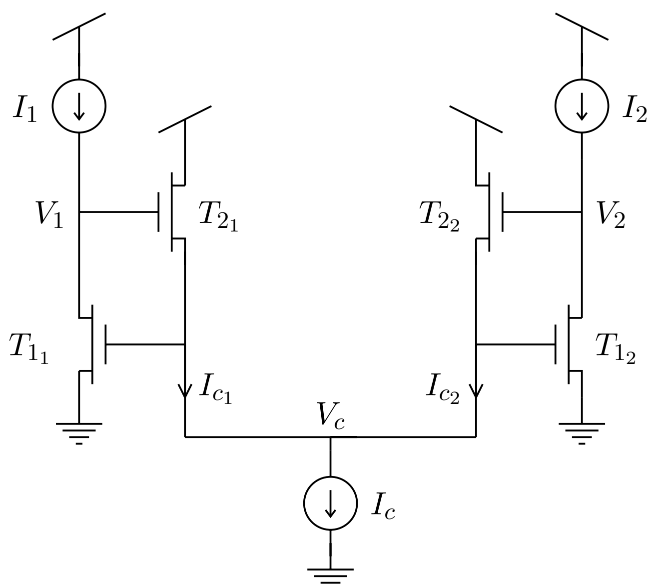

Figure 3.2. Schematic diagram of a two-neuron winner-take-all circuit.

T_{1_2} share a common gate, however; thus, T_{1_2} must also sink $I_m + \delta_i$. But only I_m is present at the drain of T_{1_2}. To compensate, the drain voltage of T_{1_2}, V_2, must decrease. For small δ_is, the Early effect decreases the current through T_{1_2}, decreasing V_2 linearly with δ_i. For large δ_is, T_{1_2} must leave saturation, driving V_2 to approximately 0 V. As desired, the output associated with the smaller input diminishes. For large δ_is, $I_{c_2} \approx 0$, and $I_{c_1} \approx I_c$. The equation $I_m + \delta_i = I_o \exp(V_c/V_o)$ describes transistor T_{1_1}, and the equation $I_c = I_o \exp((V_1 - V_c)/V_o)$ describes transistor T_{2_1}. Solving for V_1 yields

$$V_1 = V_o \ln(\frac{I_m + \delta_i}{I_o}) + V_o \ln(\frac{I_c}{I_o}). \tag{3.2}$$

The winning output encodes the logarithm of the associated input. The symmetrical circuit topology ensures similar behavior for increases in I_2 relative to I_1.

Equation 3.2 predicts the winning response of the circuit; a more complex expression, derived in Appendix 3A, predicts the losing and crossover response of the circuit. Figure 3.3 is a plot of this analysis, fit to experimental data. Figure 3.4 shows the wide dynamic range and logarithmic properties of the circuit; the experiment in Figure 3.3 is repeated for several values of I_2, ranging over four orders of magnitude.

The conductance of transistors T_{1_1} and T_{1_2} determines the losing response of the circuit. The Early voltage, V_e, is a measure of the conductance of a saturated MOS transistor. The expression

$$V_e = L\frac{\partial V_d}{\partial L} \tag{3.3}$$

defines the Early voltage, where V_d is the drain potential of a transistor, and L is the channel length of a transistor. Thus, the width of the losing response

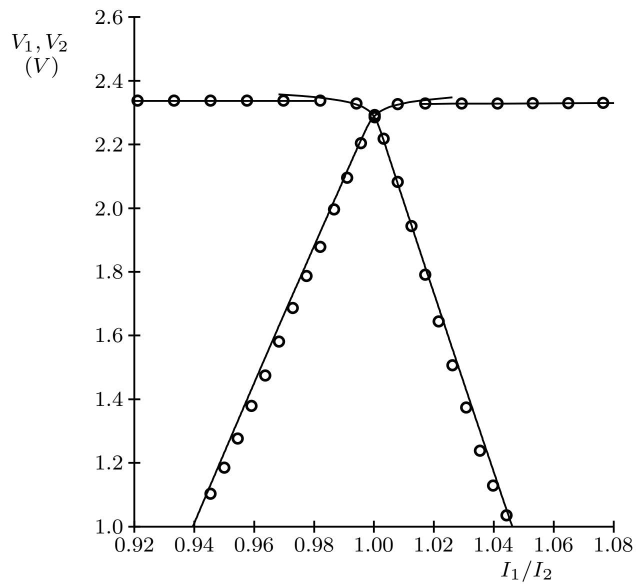

Figure 3.3. Experimental data (circles) and theoretical statements (solid lines) for a two-neuron winner-take-all circuit. I_1, the input current of the first neuron, is swept about the value of I_2, the input current of the second neuron; neuron voltage outputs V_1 and V_2 are plotted versus normalized input current.

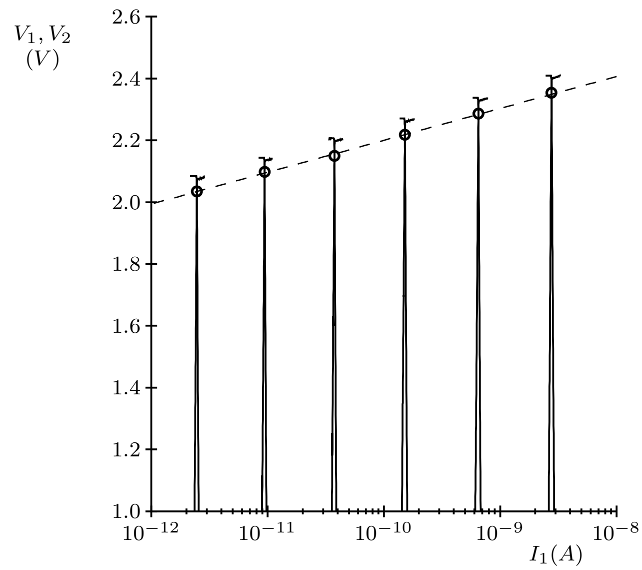

Figure 3.4. The experiment of Figure 3.3 is repeated for several values of I_2; experimental data of output voltage response are plotted versus absolute input current on a log scale. The output voltage $V_1 = V_2$ is highlighted with a circle for each experiment. The dashed line is a theoretical expression confirming logarithmic behavior over four orders of magnitude (Equation 3.1).

of the circuit depends on the channel length of transistors T_{1_1} and T_{1_2}. Figure 3.3 shows data for a circuit where the channel length of transistors T_{1_1} and T_{1_2} is 13.5 μm. Figure 3.5 shows data for a circuit with a wider losing response; in this circuit, the channel length for transistors T_{1_1} and T_{1_2} is 3 μm, the smallest allowable in the fabrication technology used.

Increasing the channel length of transistors T_{1_1} and T_{1_2} narrows the losing response of the circuit; alternatively, circuit modification also can narrow the losing response. The circuit shown in Figure 3.6 approximately halves the width of the original losing response, through source degeneration of transistors T_{1_1} and T_{1_2} by the added diode-connected transistors T_{3_1} and T_{3_2}. Figure 3.7 shows experimental data for this modified circuit.

3.2 Time Response of the Winner-Take-All Circuit

A good winner-take-all circuit should be stable, and should not exhibit damped oscillations (ringing) in response to input changes. This section explores these dynamic properties of our winner-take-all circuit, and predicts the temporal response of the circuit. Figure 3.8 shows the two-neuron winner-take-all circuit, with capacitances added to model dynamic behavior.

Appendix 3B shows a small-signal analysis of this circuit. This analysis shows that the circuit is stable and does not ring if $I_c > 4I(C_c/C)$, where $I_1 \approx I_2 \approx I$. Figure 3.9 compares this bound with experimental data.

If $I_c > 4I(C_c/C)$, the circuit exhibits first-order behavior. The time constant CV_o/I sets the dynamics of the winning neuron, where $V_o = kT/q\kappa \approx 40\,\mathrm{mV}$. The time constant CV_e/I sets the dynamics of the losing neuron, where $V_e \approx 50\,V$. Figure 3.10 compares these predictions with experimental data, for several variants of the winner-take-all circuit.

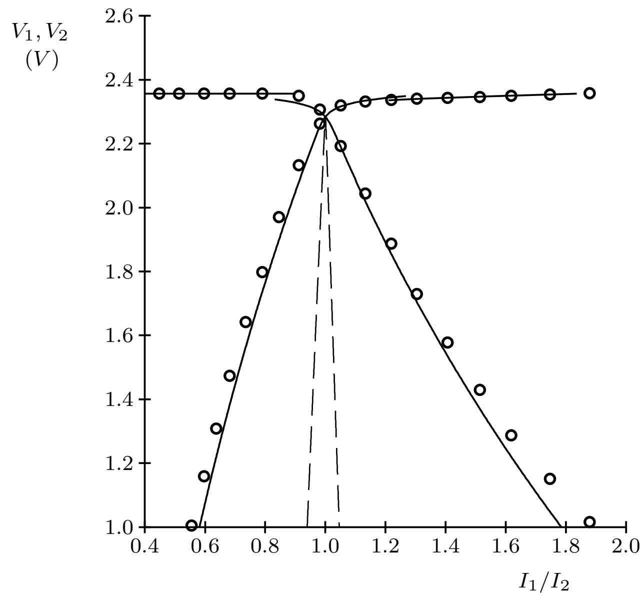

Figure 3.5. Experimental data (circles) and theoretical statements (solid lines) for a two-neuron winner-take-all circuit with a channel length for transistors T_{1_1} and T_{1_2} of $3\,\mu$m. The dotted lines show the losing response for the circuit used in Figure 3.3, which has a channel length for transistors T_{1_1} and T_{1_2} of $13.5\,\mu$m.

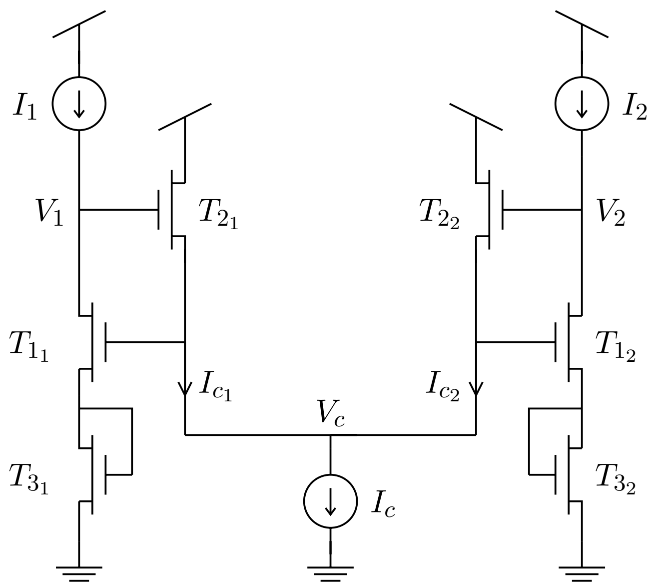

Figure 3.6. Schematic diagram of a two-neuron winner-take-all circuit, modified to produce a narrower losing response.

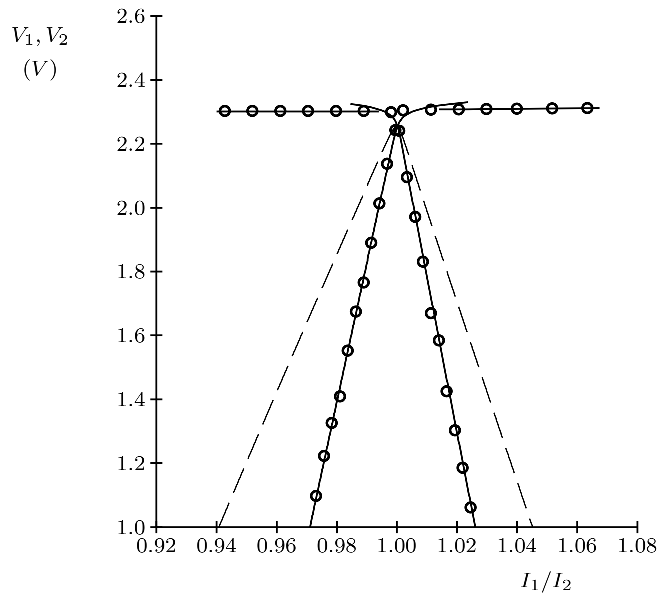

Figure 3.7. Experimental data (circles) and theoretical statements (solid lines) for a two-neuron winner-take-all circuit, modified to produce a narrower losing response. The dotted lines show losing response for the circuit used in Figure 3.4.

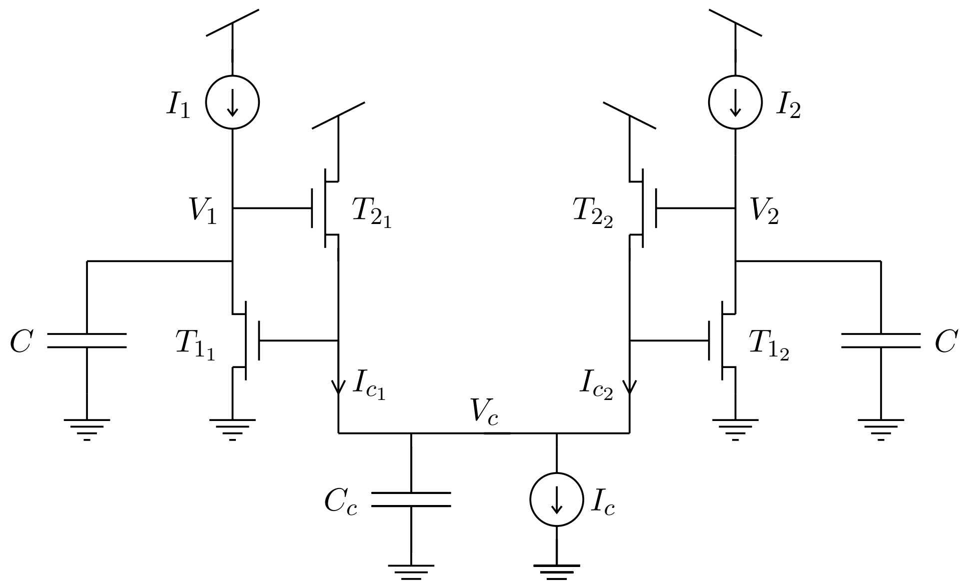

Figure 3.8. Schematic diagram of a two-neuron winner-take-all circuit, with capacitances added for dynamic analysis. C is a large MOS capacitor added to each neuron for smoothing; C_c models the parasitic capacitance contributed by the gates of T_{11} and T_{12}, the drains of T_{21} and T_{22}, and the interconnect.

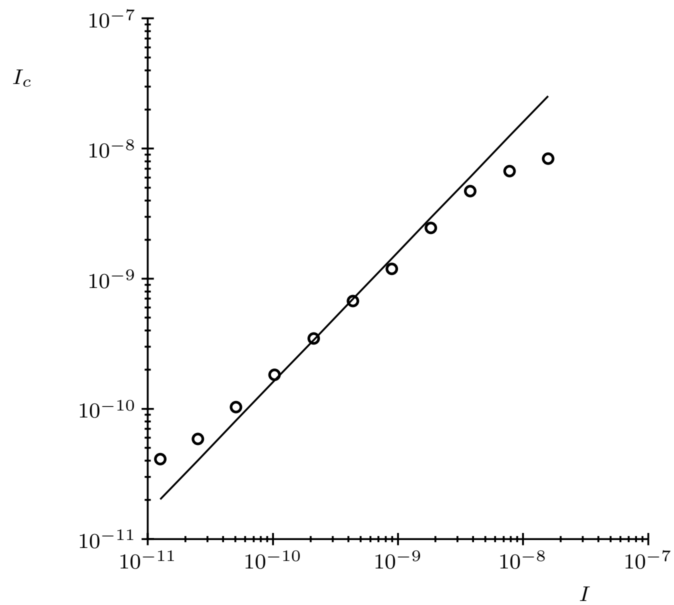

Figure 3.9. Experimental data (circles) and theoretical statements (solid line) for a two-neuron winner-take-all circuit, showing the smallest I_c, for a given I, necessary for a first-order response to a small-signal step input.

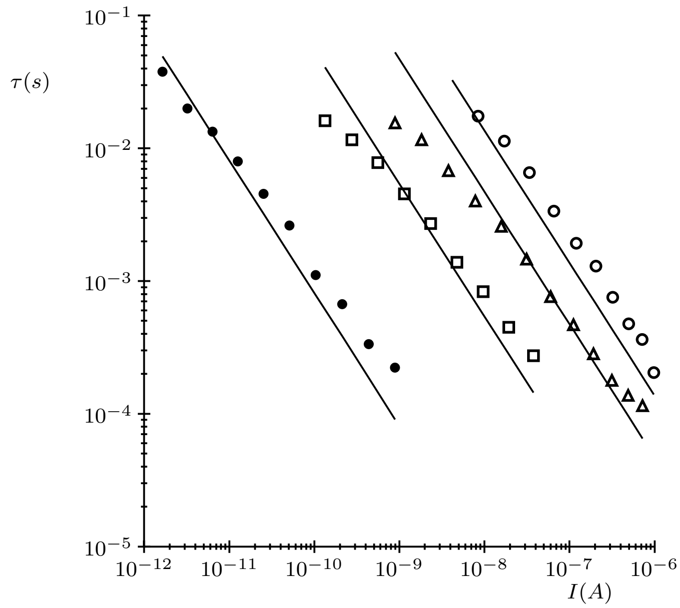

Figure 3.10. Experimental data (symbols) and theoretical statements (solid lines) for a two-neuron winner-take-all circuit, showing the time constant of the first-order response to a small-signal step input. The winning response (filled circles) and losing response (triangles) of a winner-take-all circuit with the static response of Figure 3.3 are shown; the time constants differ by several orders of magnitude. Losing responses for winner-take-all circuits with the static responses shown in Figure 3.5 (squares) and in Figure 3.7 (open circles) are also shown, demonstrating the effect of the width of static response on dynamic behavior.

3.3 The Local Nonlinear Inhibition Circuit

The winner-take-all circuit in Figure 3.1, as previously explained, locates the largest input to the circuit. Figure 3.11 shows this behavior. Figure 3.11(a) is the spatial input to a winner-take-all circuit with 16 neurons, with input 8 much higher than all other inputs. Figure 3.11(b) shows the circuit response to this input; only neuron 8 has significant response.

Certain applications require a gentler form of nonlinear inhibition. Sometimes, a circuit that can represent multiple intensity scales is necessary. Without circuit modification, the winner-take-all circuit in Figure 3.1 can perform this task. Appendix 3C explains this mode of operation.

Other applications require a local winner-take-all computation, with each winner having influence over only a limited spatial area. Figure 3.11(c) shows the desired computation. As in Figure 3.11(b), neuron 8 has the largest response in the circuit. However, neuron 8 suppresses the output of only nearby neurons; neurons far from neuron 8 have significant responses, encoding their input signals.

Figure 3.12 shows a circuit that computes the local winner-take-all function. The circuit is identical to the original winner-take-all circuit, except that each neuron connects to its nearest neighbors with a nonlinear resistor circuit (Mead, 1989). Each resistor conducts a current I_r in response to a voltage ΔV across it, where

$$I_r = I_s \tanh(\Delta V/(2V_o)). \tag{3.4}$$

I_s, the saturating current of the resistor, is a controllable parameter. The current source I_c, present in the original winner-take-all circuit, is distributed between the resistors in the local winner-take-all circuit.

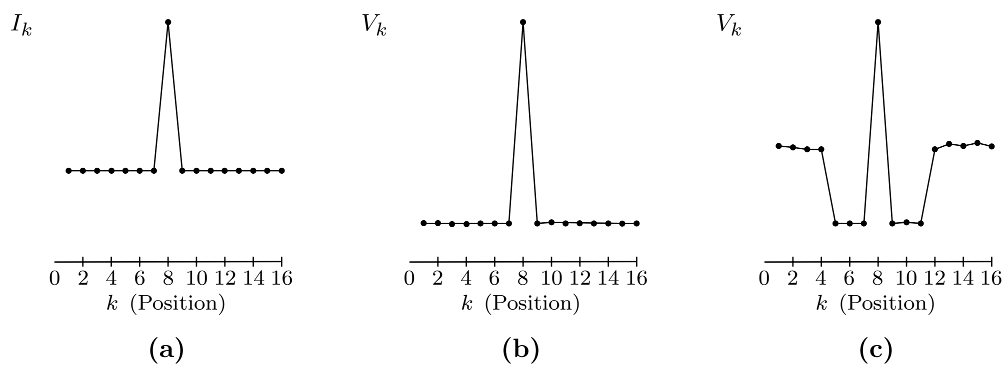

Figure 3.11. Comparison of idealized winner-take-all spatial response and the desired local winner-take-all response. The horizontal axis of each plot represents spatial position in a 16-neuron network. **a.** The plot shows a spatial impulse function, used as input to compare the two concepts. The vertical axis shows the input current to each neuron, with $I_8 \gg I_{k \neq 8}$. **b.** The plot shows the winner-take-all response. **c.** The plot shows the local winner-take-all response.

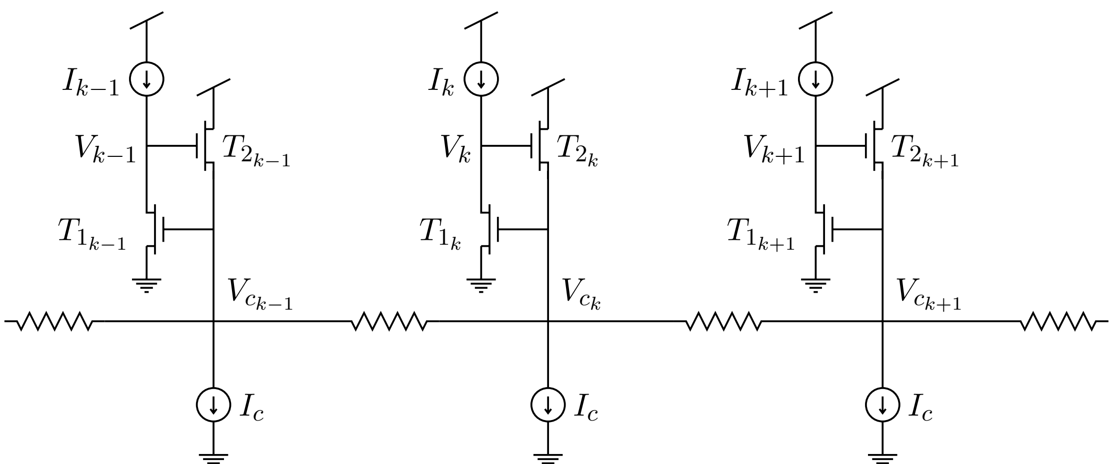

Figure 3.12. Schematic diagram of a section of the local winner-take-all circuit. Each neuron i receives a unidirectional current input I_i; the output voltages V_i represent the result of the local winner-take-all computation.

To understand the operation of the local winner-take-all circuit, we consider the circuit response to a spatial impulse, defined as $I_k \gg I$, where $I \equiv I_{i \neq k}$. $I_k \gg I_{k-1}$ and $I_k \gg I_{k+1}$, so V_{c_k} is much larger than $V_{c_{k-1}}$ and $V_{c_{k+1}}$, and the resistor circuits connecting neuron k with neuron $k-1$ and neuron $k+1$ saturate. Each resistor sinks I_s current when saturated; transistor T_{2_k} thus conducts $2I_s + I_c$ current. In the subthreshold region of operation, the equation $I_k = I_o \exp(V_{c_k}/V_o)$ describes transistor T_{1_k}, and the equation $2I_s + I_c = I_o \exp((V_k - V_{c_k})/V_o)$ describes transistor T_{2_k}. Solving for V_k yields

$$V_k = V_o \ln((2I_s + I_c)/I_o) + V_o \ln(I_k/I_o). \tag{3.5}$$

As in the original winner-take-all circuit, the output of a winning neuron encodes the logarithm of that neuron's associated input.

As mentioned, the resistor circuit connecting neuron k with neuron $k-1$ sinks I_s current. The current sources I_c associated with neurons $k-1$, $k-2$, ... must supply this current. If the current source I_c for neuron $k-1$ supplies part of this current, then the transistor $T_{2_{k-1}}$ carries no current, and the neuron output V_{k-1} approaches zero. Similar reasoning applies to neurons $k+1$, $k+2$, ... In this way, a winning neuron inhibits its neighboring neurons.

This inhibitory action does not extend throughout the network. Neuron k needs only I_s current from neurons $k-1$, $k-2$, ... Thus, neurons sufficiently distant from neuron k maintain the service of their current source I_c, and the outputs of these distant neurons can be active. Since, for a spatial impulse, all neurons $k-1$, $k-2$, ... have an equal input current I, all distant neurons have the equal output

$$V_{i \ll k} = V_o \ln(I_c/I_o) + V_o \ln(I/I_o). \tag{3.6}$$

Similar reasoning applies for neurons $k+1$, $k+2$, ...

The relative values of I_s and I_c determine the spatial extent of the inhibitory action. Figure 3.13 shows the spatial impulse response of the local winner-take-all circuit, for different settings of I_s/I_c.

3.4 Discussion

The circuits described in this chapter use the full analog nature of MOS devices to realize an interesting class of neural computations efficiently. The circuits exploit the physics of the medium in many ways. The winner-take-all circuit uses a single wire to compute and communicate inhibition for the entire circuit. Transistor T_{1_k} in the winner-take-all circuit uses two physical phenomena in its computation: its exponential current function encodes the logarithm of the input, and the finite conductance of the transistor defines the losing output response. As evolution exploits all the physical properties of neural devices to optimize system performance, designers of synthetic neural systems should strive to harness the full potential of the physics of their media.

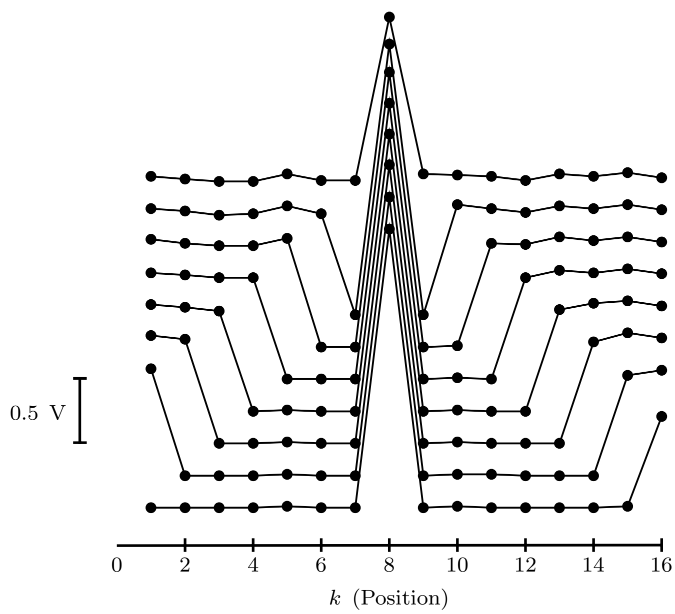

Figure 3.13. Experimental data showing the spatial impulse response of the local winner-take-all circuit, for values of I_s/I_c ranging over a factor of 12.7. Wider inhibitory responses correspond to larger ratios. For clarity, the plots are vertically displaced in 0.25 V increments.

Appendix 3A

Static Response of the Winner-Take-All Circuit

Figure 3.3 compares data from the two-neuron winner-take-all circuit with a closed-form theoretical statement describing the losing and crossover response of the circuit. This appendix derives that theoretical statement.

Figure 3A.1 shows a small-signal circuit model of the two-neuron winner-take-all circuit (Figure 3.2). For a particular operating point $[I_1, I_2, I_{c_1}, I_{c_2}]$, the model shows the effect of a small change in I_1, denoted i_1, on the circuit voltages V_1, V_2, and V_c, indicated by the small-signal voltages v_1, v_2, and v_c. In this model, a linear resistor r_{i_j}, in parallel with a linear dependent current source, with a conductance g_{i_j}, replaces each transistor T_{i_j} from Figure 3.2. For a particular operating point in subthreshold, the small-signal parameters are

$$
\begin{aligned}
g_{1_1} &= I_1/V_o, \qquad & g_{2_1} &= I_{c_1}/V_o, \qquad & r_{1_1} &= V_e/I_1, \qquad & r_{2_1} &= V_e/I_{c_1}, \\
g_{1_2} &= I_2/V_o, \qquad & g_{2_2} &= I_{c_2}/V_o, \qquad & r_{1_2} &= V_e/I_2, \qquad & r_{2_2} &= V_e/I_{c_2},
\end{aligned}
\tag{3A.1}
$$

where V_e, the Early voltage, is a measure of transistor resistance, and $V_o = kT/q\kappa$. This small-signal model is a linear system, which we can solve analytically using conventional techniques; applying the approximation $V_e + V_o \approx V_e$ to the solution yields the simplified equations

$$
\begin{aligned}
\frac{v_1}{i_1} &= (1/I_1)(V_o + V_e(I_{c_2}/I_c)), \\
\frac{v_2}{i_1} &= -V_e(1/I_1)(I_{c_1}/I_c).
\end{aligned}
\tag{3A.2}
$$

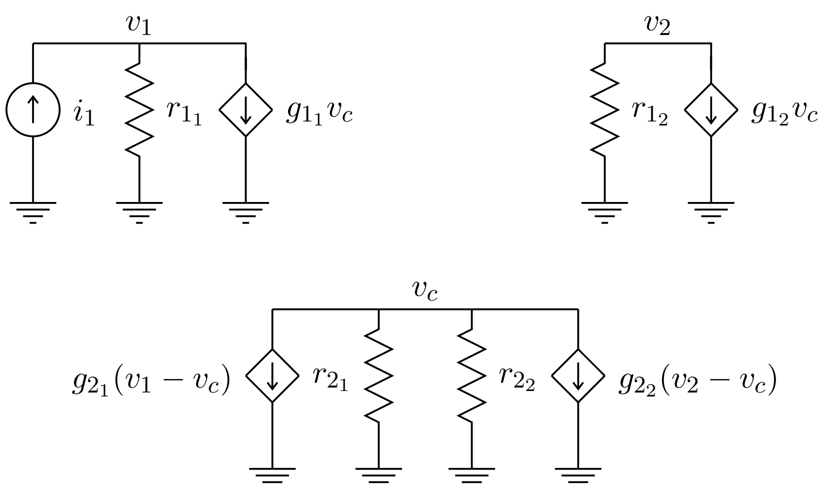

Figure 3A.1. Small-signal model of the two-neuron winner-take-all circuit.

Note that both small-signal and large-signal quantities appear in Equation 3A.2. We can view the small-signal quantities as differential elements of large-signal quantities; as a result, we can rewrite Equation 3A.2 as the pair of nonlinear differential equations

$$\begin{aligned} \frac{dV_1}{dI_1} &= (1/I_1)(V_o + V_e(I_{c_2}/I_c)), \\ \frac{dV_2}{dI_1} &= -V_e(1/I_1)(I_{c_1}/I_c). \end{aligned} \tag{3A.3}$$

Solving this pair of nonlinear differential equations yields a complete description of circuit response. We begin by eliminating I_{c_1} and I_{c_2} from the equations. Referring to Figure 3.2, the equations

$$\begin{aligned} I_{c_1} &= I_o \exp((V_1 - V_c)/V_o), \\ I_{c_2} &= I_o \exp((V_2 - V_c)/V_o) \end{aligned} \tag{3A.4}$$

describe transistors T_{2_1} and T_{2_2}. From Kirchoff's current law, we know that $I_{c_1} + I_{c_2} = I_c$; substitution of Equation 3A.4 into this equation yields the expression

$$I_c = I_o \exp((V_1 - V_c)/V_o) + I_o \exp((V_2 - V_c)/V_o). \tag{3A.5}$$

Dividing Equation 3A.4 by Equation 3A.5 eliminates V_c, leaving, after rearrangement,

$$\begin{aligned} I_{c_1}/I_c &= \frac{1}{1 + \exp((V_2 - V_1)/V_o)}, \\ I_{c_2}/I_c &= \frac{1}{1 + \exp((V_1 - V_2)/V_o)}. \end{aligned} \tag{3A.6}$$

These expressions fit nicely into Equation 3A.3, eliminating I_{c_1} and I_{c_2}, and leaving a set of differential equations involving only V_1, V_2, and I_1:

$$\frac{dV_1}{dI_1} = (1/I_1)(V_o + V_e(\frac{1}{1+\exp((V_1 - V_2)/V_o)})), \qquad (A7a)$$

$$\frac{dV_2}{dI_1} = -V_e(1/I_1)(\frac{1}{1+\exp((V_2 - V_1)/V_o)}). \qquad (A7b)$$

Equation 3A.7a contains V_2 only in the subexpression

$$\frac{1}{1+\exp((V_1 - V_2)/V_o)}; \qquad \text{(3A.8a)}$$

Equation 3A.7b contains V_1 only in the subexpression

$$\frac{1}{1+\exp((V_2 - V_1)/V_o)}. \qquad \text{(3A.8b)}$$

These subexpressions are both *Fermi functions* of the difference $V_1 - V_2$. For $V_1 - V_2 \gg V_o$, the value of the subexpression 3A.8a is approximately 0, whereas the value of the subexpression 3A.8b is approximately 1; for $V_2 - V_1 \gg V_o$, the value of the subexpression 3A.8a is approximately 1, whereas the value of the subexpression 3A.8b is approximately 0. In the region $V_1 \approx V_2$, we can assume that V_1 and V_2 are both changing with the same magnitude of slope relative to I_1. We can write this approximation as $V_1 - V_2 \approx 2(V_1 - V_m)$ and $V_2 - V_1 \approx 2(V_2 - V_m)$, where, from the qualitative analysis in the chapter, $V_m \equiv V_1 = V_2$ when $I_1 = I_2 \equiv I_m$. We can use this approximation to decouple Equations 3A.7a and 3A.7b, producing

$$\begin{aligned} \frac{dV_1}{dI_1} &= (1/I_1)(V_o + V_e(\frac{1}{1+\exp(2(V_1 - V_m)/V_o)})), \\ \frac{dV_2}{dI_1} &= -V_e(1/I_1)(\frac{1}{1+\exp(2(V_2 - V_m)/V_o)}). \end{aligned} \qquad \text{(3A.9)}$$

We can solve these equations by straightforward integration, yielding, after application of the approximation $V_e + V_o \approx V_e$,

$$\ln(I_1/I_m) = \frac{(V_1 - V_m)}{V_e} + \frac{1}{2}\ln(1 + (V_o/V_e)\exp(2(V_1 - V_m)/V_o)), \quad (3A10a)$$

$$\ln(I_1/I_m) = \frac{(V_m - V_2)}{V_e} + \frac{1}{2}(V_o/V_e)(1 - \exp(2(V_2 - V_m)/V_o)). \quad (3A10b)$$

Equation 3A.10a predicts the value of I_1 for a given value of V_1, whereas Equation 3A.10b predicts the value of I_1 for a given value of V_2; in this way, these equations are a closed-form approximation of circuit response. To understand the behavior of the circuit, and to evaluate the effect of the approximations $V_1 - V_2 \approx 2(V_1 - V_m)$ and $V_2 - V_1 \approx 2(V_2 - V_m)$, we can simplify Equations 3A.10a and 3.A10b for three regions of interest: $V_1 \approx V_2 \approx V_m$, $V_1 \gg V_m$ while $V_2 \ll V_m$, and $V_1 \ll V_m$ while $V_2 \gg V_m$.

First consider the condition $V_1 \approx V_2 \approx V_m$. In this case, $|V_1 - V_2| \rightarrow 0$, $I_1/I_m \rightarrow 1$, and we can linearize the transcendental functions in Equations 3A.10a and 3A.10b, yielding the simpler relations

$$\begin{aligned} V_1 &= (V_e/2)((I_1/I_m) - 1)) + V_m, \\ V_2 &= (V_e/2)(1 - (I_1/I_m)) + V_m. \end{aligned} \quad (3A.11)$$

In this region, V_1 and V_2 are a linear function of I_1, with a slope of $\pm V_e/(2I_m)$.

Next, consider the condition $V_1 \gg V_m$ while $V_2 \ll V_m$, valid when $I_1 > I_m$. In Equation 3A.10b, $V_2 \ll V_m$ implies $\exp(2(V_2 - V_m)/V_o) \rightarrow 0$. This simplification yields, after rearrangement,

$$V_2 = V_o/2 + V_m - V_e \ln(I_1/I_m). \quad (3A.12)$$

If we use the notation $I_1 = I_m + \delta_i$, as in the earlier qualitative analysis, we can rewrite the subexpression $\ln(I_1/I_m)$ as $\ln(1+(\delta_i/I_m))$, which we can approximate as δ_i/I_m for small δ_i/I_m, yielding the simplified result

$$V_2 = V_o/2 + V_m - (V_e/I_m)\delta_i. \tag{3A.13}$$

Thus, in this region, V_2 decreases linearly with δ_i, with a slope of V_e/I_m, which is twice as large as in the previous condition.

We can similarly derive a simplified expression for V_1, for the same condition $V_1 \gg V_m$ while $V_2 \ll V_m$. In Equation 3A.10a, $V_1 \gg V_m$ implies $(V_o/V_e)\exp(2(V_1 - V_m)/V_o) \gg 1$. This approximation yields, after rearrangement,

$$V_1 = V_o \ln(I_1/I_m) + (V_o/2)\ln(V_e/V_o) + V_m. \tag{3A.14}$$

For this condition, as predicted by Equation 3.2 in the chapter, V_1 is a logarithmic function of I_1. However, when does the approximation $(V_o/V_e)\exp(2(V_1 - V_m)/V_o) \gg 1$ hold? This inequality, when rearranged, yields the constraint

$$(V_1 - V_m) \gg (V_o/2)\ln(V_e/V_o). \tag{3A.15}$$

Therefore, for a typical fabrication process, $V_1 - V_m$ must be much greater than 0.15 V for Equation 3A.14 to hold! This error stems from the central approximation $V_1 - V_2 \approx 2(V_1 - V_m)$, which is valid for only $V_1 - V_2 \leq V_o$. Thus, for this region of operation, Equation 3.2 best predicts circuit behavior.

Finally, we consider the condition $V_1 \ll V_m$ while $V_2 \gg V_m$, valid when $I_1 < I_m$. In Equation 3A.10a, $V_1 \ll V_m$ implies $(V_o/V_e)\exp(2(V_1 - V_m)/V_o) \to 0$. This simplification yields, after rearrangement,

$$V_1 = V_m + V_e \ln(I_1/I_m). \tag{3A.16}$$

If we use the notation $I_1 = I_m - \delta_i$, as in the earlier analysis, we can rewrite the subexpression $\ln(I_1/I_m)$ as $\ln(1 - (\delta_i/I_m))$, which we can approximate as $-\delta_i/I_m$ for small $|-\delta_i/I_m|$, yielding the simplified result

$$V_1 = V_m - (V_e/I_m)\delta_i. \tag{3A.17}$$

Thus, in this region, V_1 decreases linearly with δ_i, with a slope of V_e/I_m. The losing responses for V_1 and V_2 are thus identical.

We can similarly derive a simplified expression for V_2, for the same condition $V_1 \ll V_m$ while $V_2 \gg V_m$. For Equation 3A.10b, $V_2 \gg V_m$ implies $\exp(2(V_2 - V_m)/V_o) \gg 1$. This approximation yields, after rearrangement,

$$\ln(I_1/I_m) = (V_m - V_2)/V_e - (1/2)(V_o/V_e)\exp(2(V_2 - V_m)/V_o). \tag{3A.18}$$

As $V_2 - V_m$ increases, the right side of this equation grows exponentially large and negative, forcing I_1 to grow closer and closer to zero; thus, V_2 is constant with I_1. However, the poor approximation $V_2 - V_1 \approx 2(V_2 - V_m)$ for $V_2 - V_1 \geq V_o$ stunts this exponential growth. The qualitative analysis in the chapter predicts this constant value accurately, as

$$V_2 = V_o \ln(\frac{I_m}{I_o}) + V_o \ln(\frac{I_c}{I_o}). \tag{3A.19}$$

In summary, Equations 3A.10a and 3A.10b predict the losing and crossover response of the circuit, whereas Equations 3.2 and 3A.19 predict the winning response of the circuit. Figure 3.4 is a plot of this analysis, fitted to experimental data. Figure 3A.2 expands the crossover region of Figure 3.4, showing the crossover region between losing and winning analyses. The theoretical predictions in Figure 3.5 and Figure 3.7 also use this analysis, with altered values of V_e.

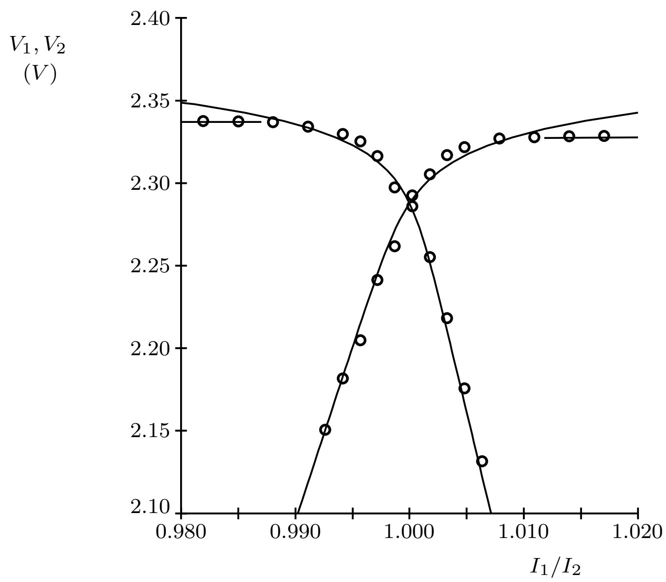

Figure 3A.2. Experimental data (circles) and theoretical statements (solid lines) for a two-neuron winner-take-all circuit in the crossover region.

Appendix 3B

Dynamic Response of the Winner-Take-All Circuit

In the chapter, we presented theoretical predictions of the time response of the winner-take-all circuit; in Figure 3.9 and 3.10, we compared these predictions with experimental data. In this appendix, we derive these theoretical predictions.

Figure 3.8 in the chapter shows a schematic diagram for a two-neuron winner-take-all circuit, with capacitances added to model dynamic behavior. Figure 3B.1 shows a small-signal circuit model for this circuit. For a particular operating point $[I_1, I_2, I_{c_1}, I_{c_2}]$, the model shows the effect of a small change in I_1, denoted by i_1, on the circuit voltages V_1, V_2, and V_c, indicated by the small-signal voltages v_1, v_2, and v_c. In this model, a linear resistor r_{i_j}, in parallel with a linear dependent current source, with a conductance g_{i_j}, replaces each transistor T_{i_j} from Figure 3.2. For a particular operating point in subthreshold, the small-signal parameters are

$$\begin{aligned} g_{1_1} &= I_1/V_o, & g_{2_1} &= I_{c_1}/V_o, & r_{1_1} &= V_e/I_1, & r_{2_1} &= V_e/I_{c_1}, \\ g_{1_2} &= I_2/V_o, & g_{2_2} &= I_{c_2}/V_o, & r_{1_2} &= V_e/I_2, & r_{2_2} &= V_e/I_{c_2}, \end{aligned} \tag{3B.1}$$

where V_e, the Early voltage, is a measure of transistor resistance, and $V_o = kT/q\kappa$. This small-signal circuit model is a linear system, which we can solve analytically using conventional techniques. The resulting solution, unfortunately, is a function of the unsolved large signal I_{c_1} and I_{c_2}. However, for the input conditions $I_2 = I_m$ and $I_1 = I_m + \delta_i$, we can reasonably make the approximations $I_{c_1} \approx I_c$ and $I_{c_2} \approx 0$ for relatively small δ_i, due to the exponential dependence of T_{21} and T_{22} on V_1 and V_2. Using these approximations, we can express the small-signal voltages v_1 and v_2 as linear functions of the small-signal input current i_1, as

$$\frac{v_1}{i_1} = (\frac{V_o}{I_1})\frac{((C_cV_o/I_c)s+1)}{(s/(a+b)+1)(s/(a-b)+1)} \tag{3B.2}$$

and

$$\frac{v_2}{i_1} = -(\frac{V_e}{I_1})\frac{1}{((CV_e/I_2)s+1)(s/(a+b)+1)(s/(a-b)+1)}, \tag{3B.3}$$

where

$$a = \frac{I_1}{2CV_e} + \frac{I_c}{2C_cV_o} \tag{3B.4}$$

and

$$b = \sqrt{(\frac{I_1}{2CV_e})^2 + (\frac{I_c}{2C_cV_o})^2 - (\frac{I_cI_1}{CC_cV_o^2})}. \tag{3B.5}$$

If b is an imaginary number, the circuit has complex poles, and exhibits undesirable ringing behavior. If $I_c > 4I_1(C_c/C)$, then b is real, and ringing does not occur. Figure 3.9 in the chapter compares experimental data with this inequality.

When b is real, the circuit exhibits first-order behavior. We can simplify Equations 3B.2 and 3B.3, and show that the first-order time constant for V_1 is CV_o/I, and the first-order time constant for V_2 is CV_e/I, where $I_1 \approx I_2 \equiv I$. Figure 3.10 in the chapter compares experimental data with these time constants.

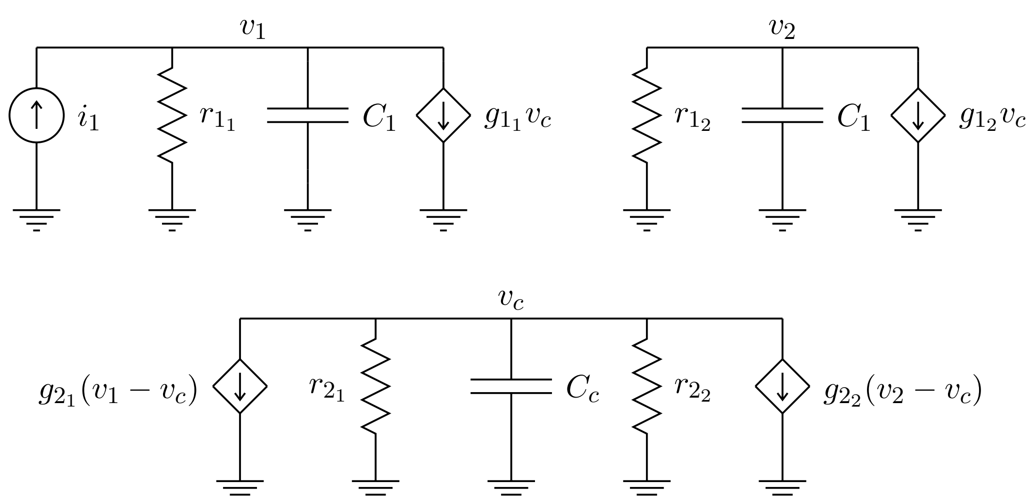

Figure 3B.1. Small-signal model of the two-neuron winner-take-all circuit, with capacitances added to model dynamic behavior.

Appendix 3C

Representation of Multiple Intensity Scales

This appendix explains a regime of operation of the winner-take-all circuit that represents multiple input intensity scales in the output, while still functioning as an inhibitory circuit.

Consider an n-neuron winner-take-all circuit, with input currents $I_1 \gg I_2 \gg \ldots \gg I_n$. As shown in Equation 3.1 in the chapter, the output voltage V_1 is

$$V_1 = V_o \ln(\frac{I_1}{I_o}) + V_o \ln(\frac{I_c}{I_o}), \tag{3C.1}$$

while $V_2 \ldots V_n$ are approximately zero. The output does not represent the input ordering $I_2 \gg I_3 \gg \ldots \gg I_n$; the largest input wins, and all other inputs lose. We can operate the circuit in another regime, however, which allows inputs $I_1 \ldots I_k$ to win, and inputs $I_{k+1} \ldots I_n$ to lose, where the magnitude of I_k is under external control. Voltage outputs $V_1 \ldots V_{k-1}$ are now binary representations, whereas V_k maintains a logarithmic encoding of the input current I_k.

In our previous analysis in the chapter, we used ideal current sources to represent $I_1 \ldots I_n$. In Figure 3C.1, we replace these ideal sources with transistor realizations. Transistors $T_{3_1} \ldots T_{3_n}$, when operating in the subthreshold region, realize ideal current sources if $V_{dd} - V_k > 2V_o$. Recall our input $I_1 \gg I_2 \gg \ldots \gg I_n$, and consider the effect of increasing the value of current source I_c. As shown in Equation 3C.1, the neuron output V_1 increases with I_c. For large I_c, transistor T_{2_1} is no longer operating in the subthreshold region. In this case, the equation $I_{c_1} = k'(W/L)(V_1 - V_c - V_T)^2$ describes T_{2_1}, where W and L are the width and length of T_{2_1}, and k' and V_T (the threshold voltage) are fabrication constants. We can solve for V_1 for this situation, as

$$V_1 = V_o \ln(\frac{I_1}{I_o}) + \sqrt{\frac{I_c}{k'(W/L)}} + V_T. \tag{3C.2}$$

If we increase I_c further, V_1 continues to increase. For a sufficiently large I_c, V_1 can approach V_{dd}. In this situation, T_{3_1} begins to turn off, and no longer acts as an ideal current source supplying I_1. In this case, we can model T_{2_1} as an independent current source, supplying the current $I_s \equiv k'(W/L)(V_{dd} - V_c)^2$, as shown in Figure 3C.2. To a first approximation, Figure 3C.2 shows a winner-take-all circuit with $(n-1)$ neurons, with an effective control current of $I_c - I_s$.

We can apply this technique to represent multiple input intensity scales. Recall the input condition $I_1 \gg I_2 \gg \ldots \gg I_n$, and the desired behavior of outputs: $V_1 \ldots V_{k-1}$ to be approximately V_{dd}, V_k to maintain a logarithmic encoding of the input current I_k, and all other output voltages to be approximately 0. To produce this behavior, we simply increase I_s, until $V_1 \ldots V_{k-1}$ are approximately V_{dd}, but $V_k < V_{dd}$.

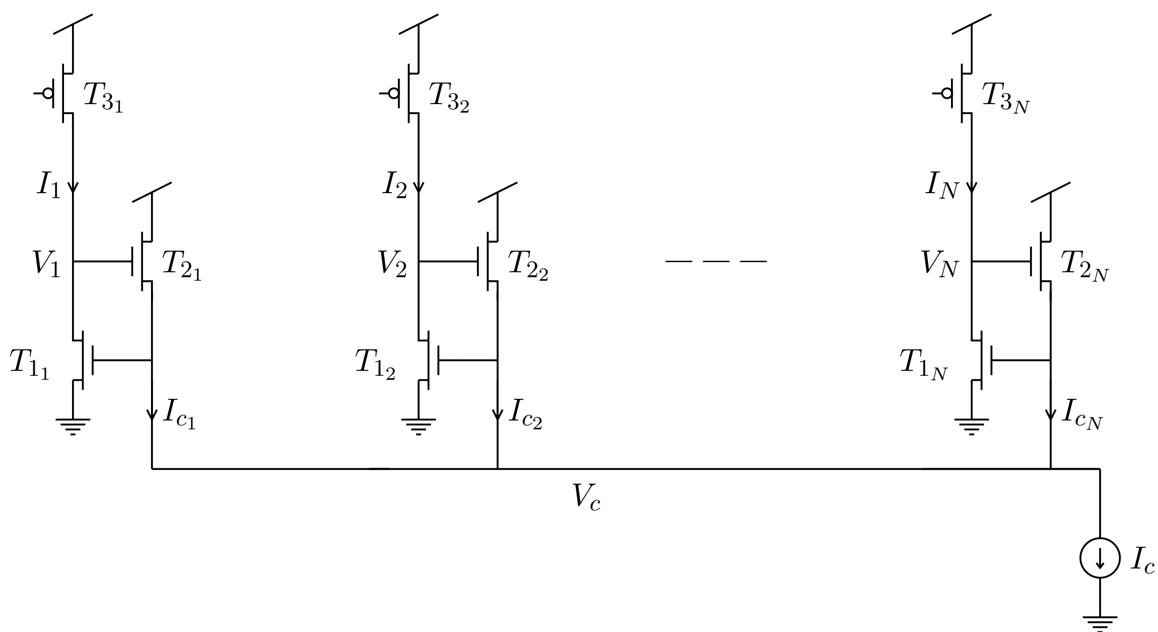

Figure 3C.1. Winner-take-all circuit, with transistor realizations replacing ideal input current sources.

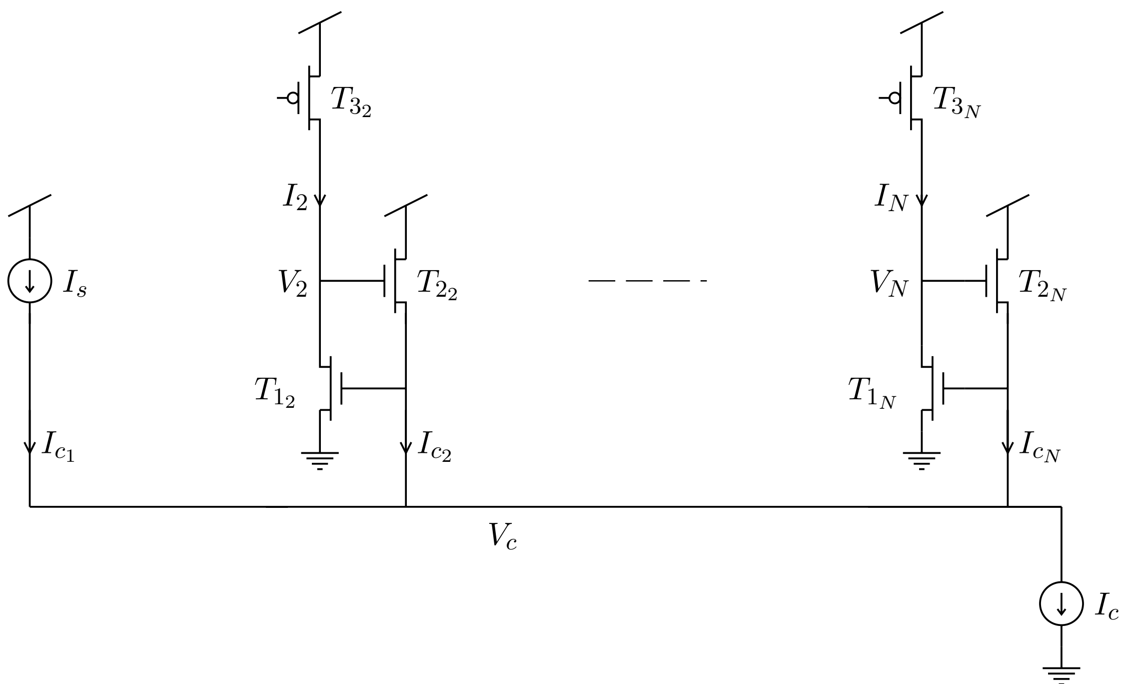

Figure 3C.2. Winner-take-all circuit, after modeling a saturated neuron with the independent current source I_s.