Low-Power Silicon Spiking Neurons and Axons

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Abstract

This paper presents low-power versions of two circuits often used in analog VLSI models of neural systems. The circuits model the spiking behavior of the axon hillock and the pulse propagation of axons.

1 Introduction

As device dimensions decrease, die sizes increase, and wafer-scale techniques mature, power consumption becomes a dominant issue in VLSI system design. A silicon neural design style that operates MOS transistors in the weak-inversion regime [7] [1] supports low-power VLSI design. In this design style, popular circuits that model continuous-time dendritic processing operate all transistors in the weak-inversion regime. In contrast, several popular circuits in this design style, that model the spiking behavior of the axon hillock and the pulse propagation of axons, operate several transistors outside the weak-inversion regime. In many neural implementations, these axon circuits dominate power consumption [3] [4] [5] [6] [2].

I have designed, fabricated, and tested versions of these axon circuits; in these modified circuits, all transistors operate in the weak-inversion regime. The modified circuits are fully functional, and show a measured improvement in power consumption over the original circuits. Power consumption decreases of a factor of 10 to 1000 have been measured, depending on pulse width and spiking frequency.

The density of the modified circuits is comparable to the original circuits. The modified axon hillock circuit adds one transistor to the original circuit; the modified model of axonal pulse propagation adds one transistor to each stage of delay of the original circuit. The modified circuits also add two control voltages to the original circuits; judicious use of a process with two layers of polysilicon allows the addition of these wires with a minimal increase in density.

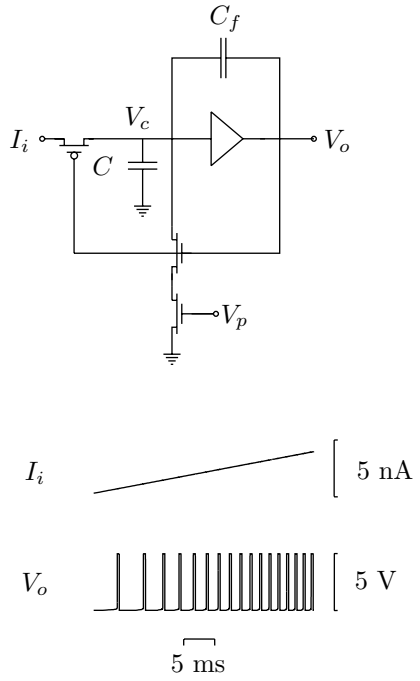

Figure 1: Spiking neuron circuit and function, with unidirectional current input I_i, voltage pulse output V_o, and pulse width control voltage V_p.

2 Circuit Details

Figure 1 shows the spiking neuron circuit from [7], that uses a high-gain voltage amplifier with a sigmoidal nonlinearity as a gain element. The circuit converts the unidirectional current I_i into a sequence of fixed-width, fixed-height voltage pulses of V_o. During a pulse $V_o = V_{dd}$, and between pulses V_o is at ground potential.

To understand circuit operation, consider the circuit condition after an output pulse has completed. In

this state, V_o is at ground potential, and V_c is lower than the switching threshold of the amplifier. The discharge path of the state capacitor C is closed, and the charging path of C is open.

The circuit remains in this state until the input current I_i increases V_c to the switching threshold of the amplifier. At this point, V_o switches to V_{dd}. The feedback capacitor C_f ensures the secure switching of the circuit. The new value of V_c is above the switching threshold of the amplifier, and depends on the relative values of C_f and C.

Once a pulse begins, the discharge path of the state capacitor C is open, and the charging path of C is closed. The control voltage V_p sets the discharge rate of C, and thus the width of voltage pulse of V_o. The circuit remains in this state until V_c decreases to the switching threshold of the amplifier. At this point, V_o switches to ground potential, and the pulse is complete. The voltage V_c is reset to a value below the switching threshold of the amplifier, that depends on the relative values of C_f and C.

This circuit, as described in [7], uses two digital inverters in series as the high-gain amplifier; Figure 2 (top) shows this amplifier implementation. When used in the spiking neuron circuit, the transistors in first inverter of this amplifier are biased outside the weak-inversion regime. In many designs, the static current consumption of these transistors dominates the current consumption of the chip.

Figure 2 (bottom) also shows a low-power implementation of a high-gain amplifier suitable for use in the spiking neuron circuit. The control voltages K_1 and K_2 limit the static current consumption of the amplifier. The response time of the amplifier is not symmetric; the speed of crossing the amplifier threshold in a positive direction is not limited by K_1 and K_2, but the speed of crossing the amplifier in a negative direction is directly dependent on K_1 and K_2. In many applications, this asymmetry allows the bias currents of the amplifier to be set in the weak-inversion regime. The diode-connected transistor acts to raise the switching threshold of the amplifier.

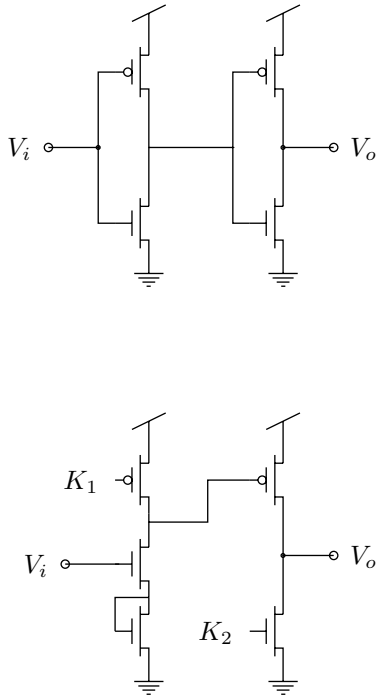

Figure 2: Original gain stage (top circuit) and low-power gain stage (bottom circuit). K_1 and K_2 are control voltages, set to ensure all transistors operate in the weak-inversion regime.

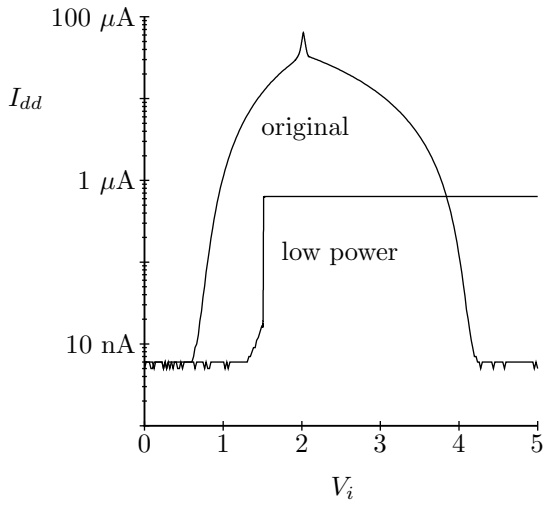

Figure 3: Power supply current I_{dd} for original gain stage and low-power gain stage, as a function of V_i. Note log scale for current.

3 Experimental Data

Figure 3 shows the static current consumption of the two amplifiers shown in Figure 2, as a function of the input voltage V_i. This figure shows data from a test chip fabricated in the 2μm double polysilicon n-well Orbit process as supplied by MOSIS. The current meter used in this measurement is not able to measure

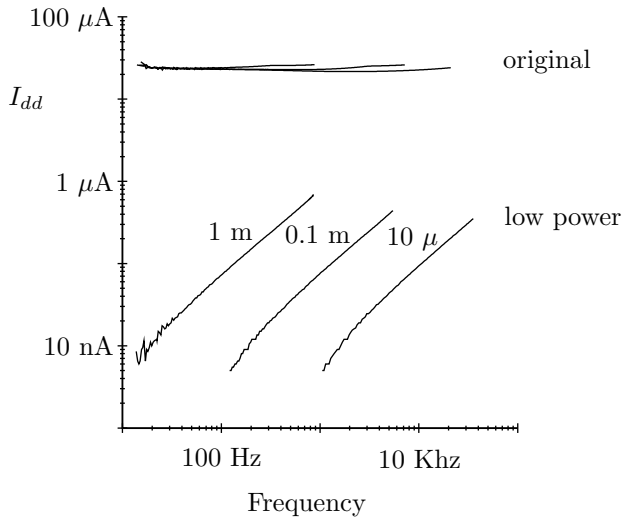

Figure 4: Power supply current I_{dd} for original spiking neuron circuit and low-power spiking neuron circuit, as a function of spiking frequency. Labels next to graphs indicate pulse width of spikes, in units of seconds. Note log scale for frequency and current.

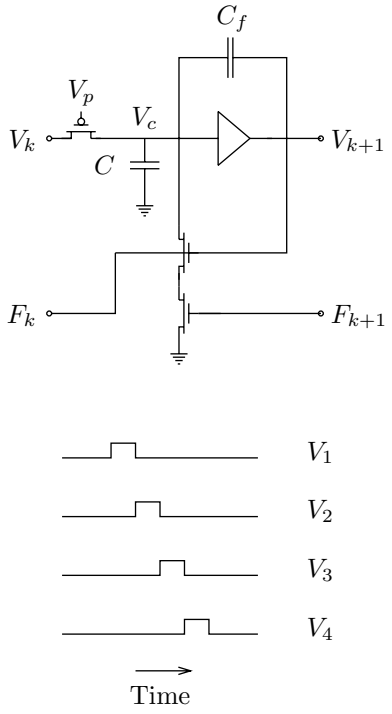

Figure 5: Axon circuit and function. Labels include ports V_k and F_k to previous stage, ports V_{k+1} and F_{k+1} to next stage, pulse width control voltage V_p, state voltage V_c, state capacitor C and feedback capacitor C_f.

currents below 5 nA. As expected, the low-power amplifier consumes negligible current below its switching threshold, and a constant current above its switching threshold.

Figure 4 shows the current consumption of the spiking neuron circuit of Figure 1, implemented with the original amplifier and the low-power amplifier. As expected, the current consumption of the low-power circuit is a linear function of spiking frequency, and increases with the size of the pulse width. All data was taken with the values of K_1 and K_2 necessary for correct circuit function with 10μs pulses; the current consumption for longer pulse-width operation can be reduced by adjusting K_1 and K_2.

4 The Axonal Delay Circuit

Figure 5 shows one section of the axonal delay line circuit described in [7]. In engineering terms, the circuit is a cascade of non-retriggerable monostables, each with a voltage output V_k, that is either at V_{dd} or at ground potential. To understand circuit operation, consider the condition $V_k = V_{dd}$, $V_{k+1} = 0$, $F_{k+1} = 0$. In this case, the voltage V_c as shown in Figure 5 is below the switching threshold of the amplifier. The discharge path of the capacitor C is closed, and C is charged by a current set by the voltage $V_k - V_p \equiv V_{dd} - V_p$. When the voltage V_c increases to the switching threshold of the amplifier, V_{k+1} changes to V_{dd}, and the axon stage associated with V_{k+2} begins a similar charging cycle. Once this cycle has completed, the voltage F_{k+1} switches to V_{dd} and the capacitor C associated with V_{k+1} quickly discharges, causing the voltage V_{k+1} to switch back to ground. In this way, a constant width voltage pulse propagates down the structure.

As with the spiking neuron circuit, the amplifier in each neuron circuit, if implemented with two digital inverters in series, consumes appreciable static current. Replacing the original amplifier with the low-power amplifier reduces the current consumption of an axonal delay circuit. Figure 6 shows the current consumption of an 18-stage axonal delay circuit, implemented with the original amplifier and the low-power amplifier.

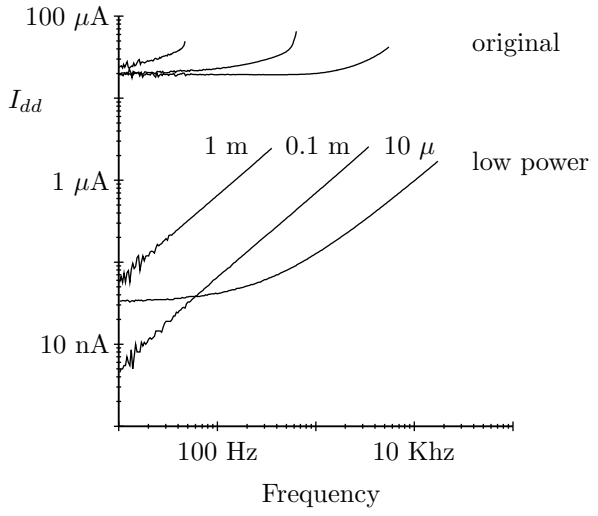

Figure 6: Power supply current I_{dd} for original axon circuit and low-power axon circuit, as a function of spiking frequency (18 sections). Labels next to graphs indicate pulse width of spikes, in seconds. Note log scales for current and frequency.

For pulse widths of 100 μs and 1 ms, current consumption of the low-power axon circuit is a linear function of spiking frequency. For a pulse width of 10 μs, the state capacitors C are not fully discharged with a single pulse, and some additional static current consumption occurs. As with the spiking neuron circuit, the current consumption of the low-power axon circuit also depends on pulse width length. All data was taken with the values of K_1 and K_2 necessary for correct circuit function with 10μs pulses; the current consumption for longer pulse width operation can be reduced by adjusting K_1 and K_2.

The original axon circuit has a single free parameter, V_p, that sets both the speed of pulse propagation and the width of each pulse. The low-power axon circuit provides two additional parameters, K_1 and K_2. These parameters permit the pulse width and propagation speed to be set independently, allowing overlapping pulses in successive taps.

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